

# CHALLENGE THE EXPERT:

## Solving the Complexity Challenge in the Design of Electronic Systems

Silicon Valley World Internet Center

March 20, 2003

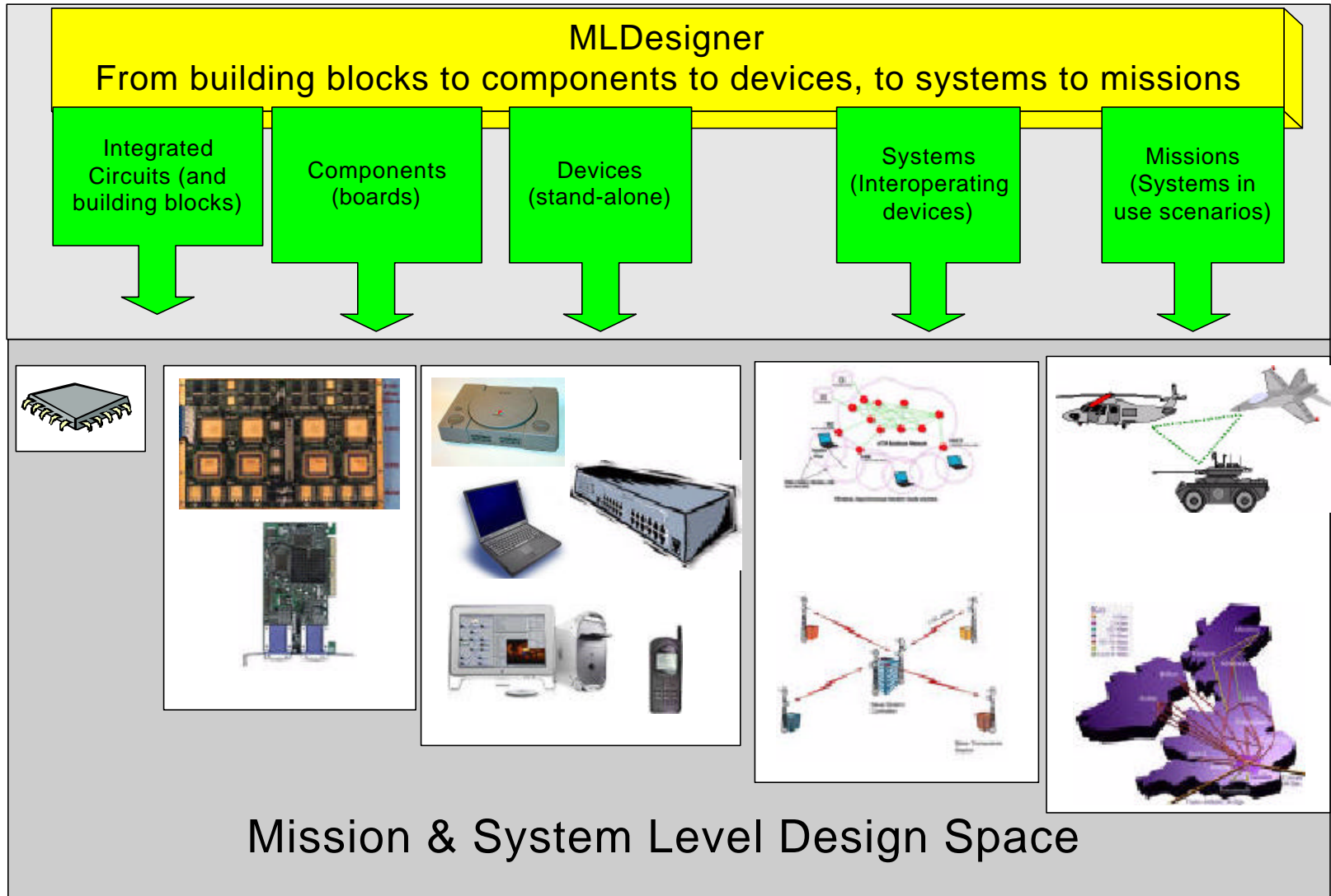
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# Electronic Design Challenge: Complexity

The complexity doubles doubles every 1.5 years or goes up by a factor 100 every 10 years

- 1970s: Physical Design: CAD
- 1980s: Logic Level Design, Verilog, VHDL increased the productivity of design engineers and made the design of complex electronic systems possible
- 1990s: Functional level design:
  - *Cadence* bought *Comdisco Systems* to get the tool **SPW**
  - *Synopsys* bought *Cadis* to get the tool **COSSAP**
  - *Mentor* partners with *Imec* to get the tool **DesignStation**

# MLDesigner Design Space

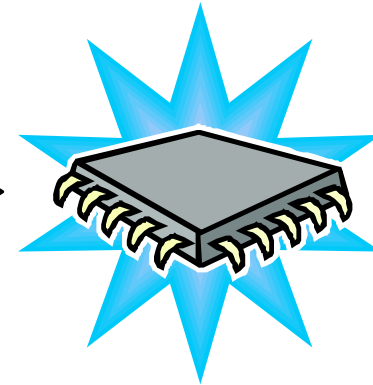
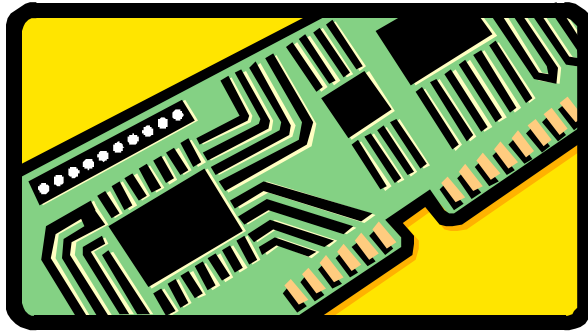


# Common Characteristics

- Architectural Complexity
  - Concurrent processing (hardware & software)
  - Contention for shared resources (CPU, memory, channels, disk, etc)
- Dynamic Interactions between Subsystems
  - Performance dictated by channel protocols (e.g. arbitration policies, transfer modes, co-channel interference, collisions)
  - Static analysis techniques like queuing theory ignore channel contention – providing theoretical upper bound on performance (poor predictive value for architectural tradeoffs)
- Complex Functionality
  - Validation of complex algorithms and protocols is essential
  - Quantitative and/or qualitative performance dictated by algorithmic tradeoff studies

# The Trend: Complexity

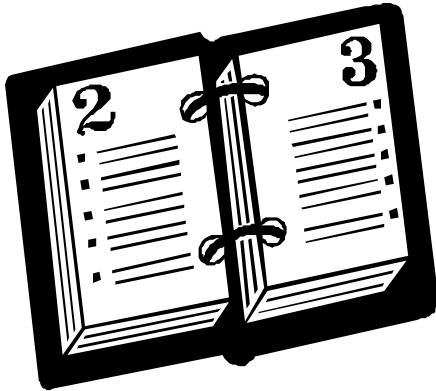
- “System-on-chip” Integration and Time-to-market
  - 2000th: Electronic systems are again 100 times more complex than in the 1990th
  - Time-to-market and product lifespan have shrunk



- Dataquest: In 2005 50% of designs will be done with Next generation electronic system-level design (SLD) tools and design flow methodology
- Infineon: without SLD, 10,000x improvement in current EDA tools required by 2003 to keep pace with semi tech.

Sources: Gary Smith of Gartner Dataquest; Keynote Address at DATE 2001 Conference

# Problem 1: Simulation Speed



**Simulations must be measured  
In Hours, not Days!**

## Cycle-Accurate Models

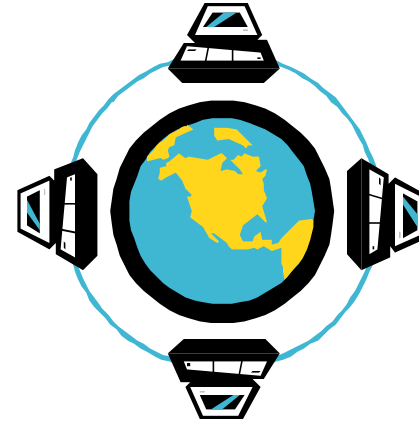
- ✓ ok for detailed hardware design
- ✓ ok for software profiling
- ✓ ok for debugging HW/SW interfaces
- TOO SLOW for architectural tradeoffs
- TOO SLOW for predicting application performance

# Problem 2: Broken Processes

Incompatible System-Level  
Tools and Models



Multiple Development Sites  
And Companies

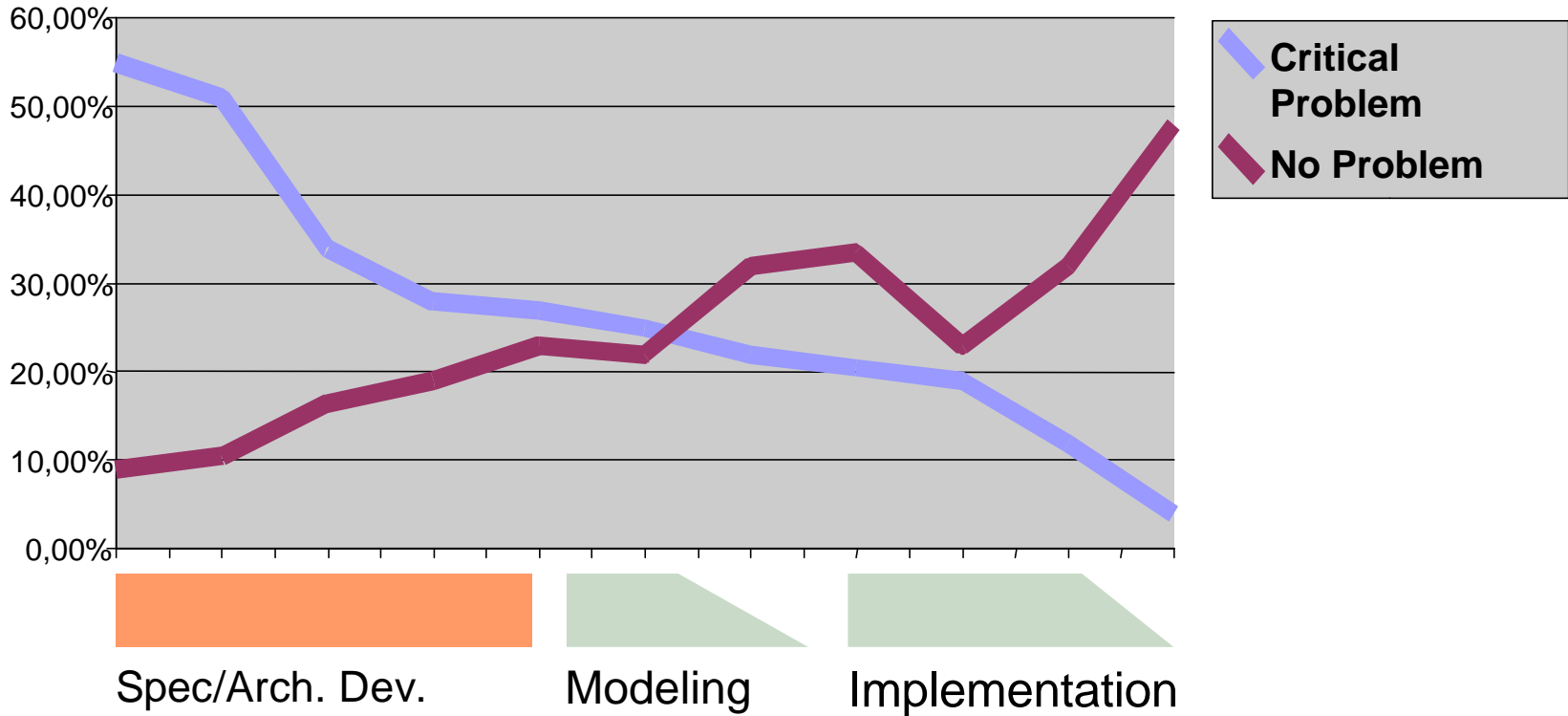


*The Impact: Expensive Problem Solving Late in Design Cycle*

- Can't predict performance of interacting subsystems
- Can't predict performance in context of operational environment
- Can't deliver architectural performance models to end customer
- Expensive rework to fix system-level problems after first prototype
- Difficult to share and reuse system-level models

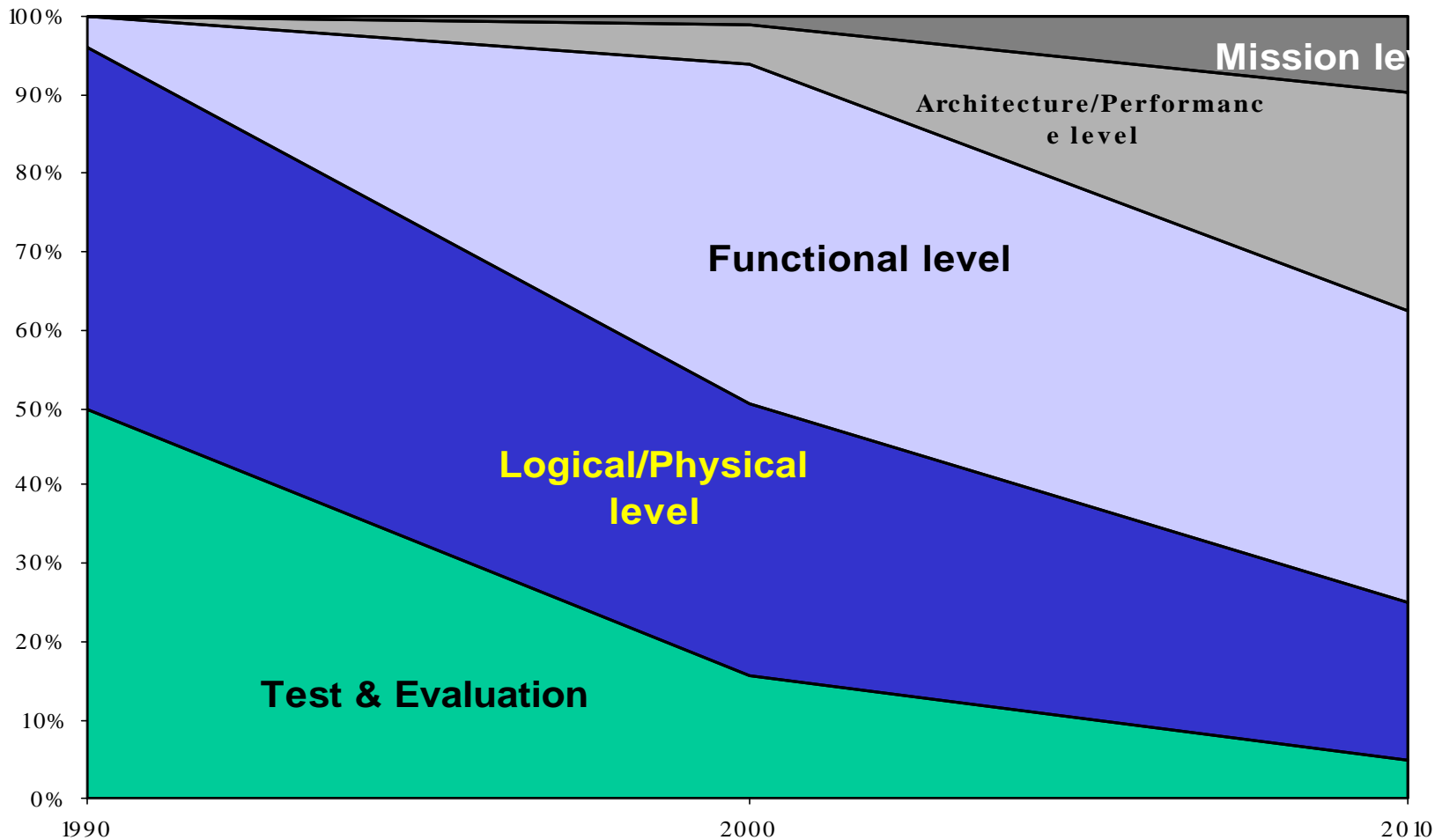
# HW/SW Problems Due to Complexity

ESPITI Study



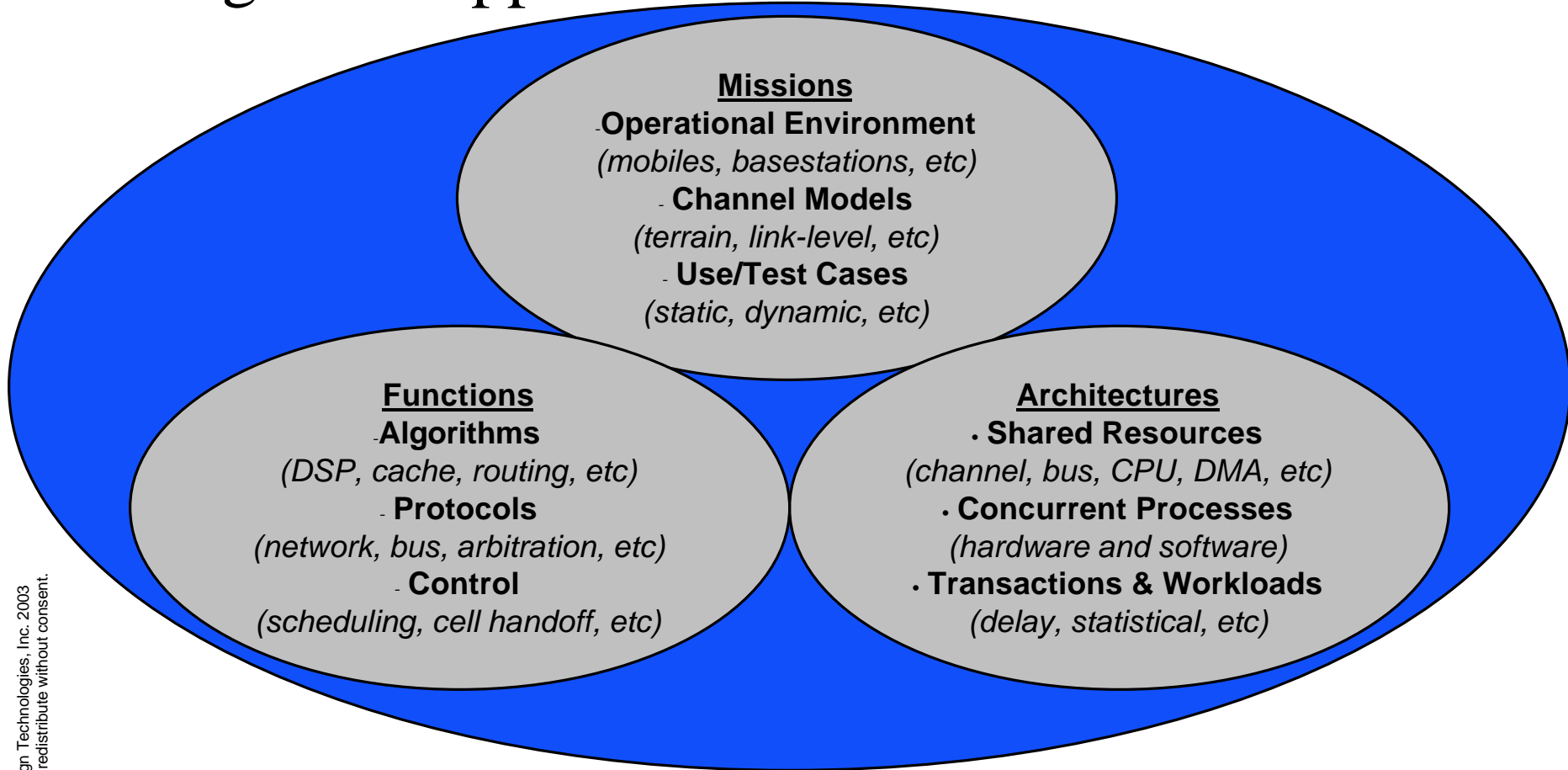
➔ The main problem is spec/architecture development

# The Solution, Part 1: Raise Abstraction Level



# The Solution, Part 2:

## Integrated Approach for HW and SW

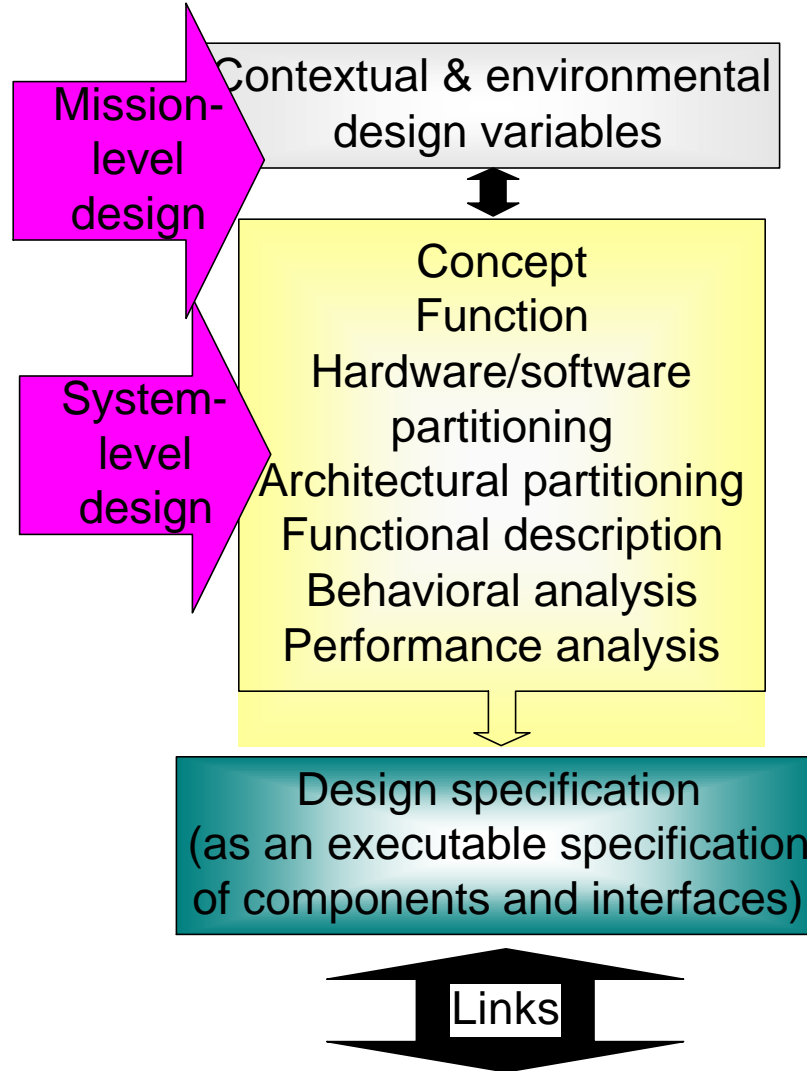


*Next Generation System Design Requires  
An Integrated Approach, Not Point-Tools*

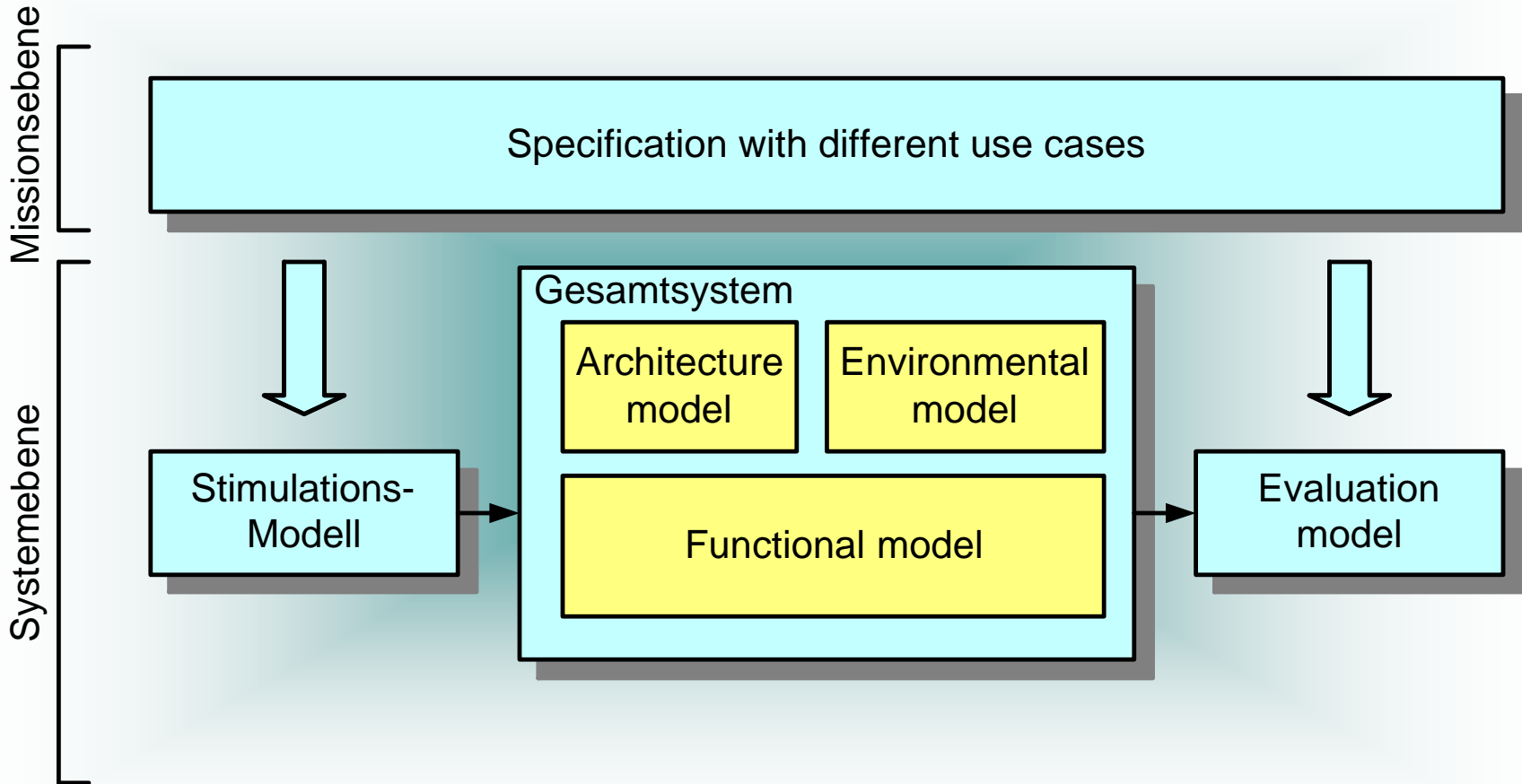
# Integrated Environment

- Standardized design environment and language to capture Architectures, Functions and Missions
- Tools for analysis and tradeoff studies of:
  - Concept development/ Mission level test environment
  - Architectural performance
  - HW/SW partitioning
  - Functional performance

# System/Mission level design



# Integrated Simulation at System Level



MLDesigner...0], Copyright (c) 2003 MLDesign Technology ...Mgraph.input=4#1 : QR Utilization TimeAverageStatistics (Capacity, Max, Mean, Min)

File Edit View Window Settings

ActiveReadQuantityResource [file:\$MLD/MLD\_Lit

Name Domain

- MLD Examples
  - Aloha
  - BitErrorRate
  - CpuDemo
    - Cpu DE
    - CpuSystem DE
    - PacketSource DE
    - StatisticsReporter DE
- Demos
- Emergency Radio
- Medical Network Demo
- Mobile Radio

Name Value

CPUResol.

Name	CPUResource
Type	Server
Scope	Internal
Description	
Number of Dim...	1
Initial Number ...	10
Initial Service ...	1.0
Server Mecha...	Dedicated_Server
Maximum Docu...	100
Context Switc...	0.01
Preempt Discip...	Allow_Preemption
Queue Discipline	First_In_First_Out
Queue Reject ...	Incoming_DS_Rejected

System Properties Resource Properties

QR Utilization TimeAverageStatistics (Capacity, Max, Mean, Min)  $\times 10^5$

Capacity Max Mean Min

SR ServerUtilization TimeAverageStatistics (Capacity, Max, Mean, Min)  $\times 10^3$

Capacity Max Mean Min

Save EPS... Print Fill Close Close All

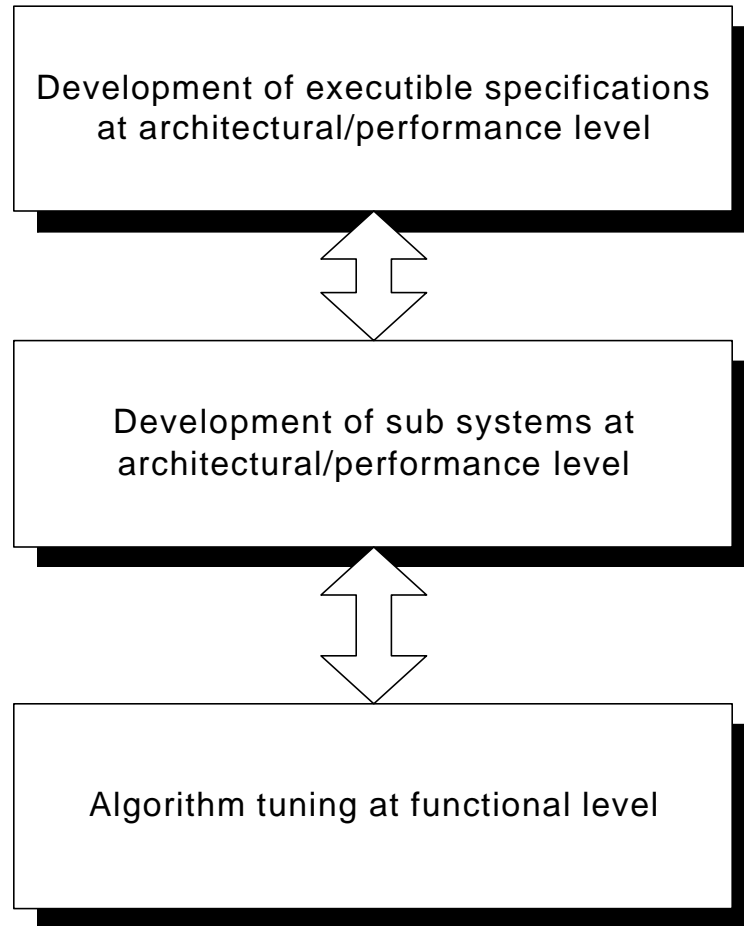
MemoryResource CPUResource

PacketSource [Priority 0] Select Length AllocateBasic#1 Cpu#1 Select Length FreeBasic#1 StatisticsReporter#1

PacketSource [Priority 1] Display Msg#1

Hold mouse and drag to select rectangular region. Use Ctrl for additional option. Alt - Zoom, Space - Pan [-303, -167]

# Design flow for complex systems



# MLDesigner

- MLDesign has developed **MLDesigner**, which supports the complete system level design flow from specification development to implementation handoff
- This includes
  - Specification development of Hardware and Software + architecture/performance trade-off before detailed design
  - Functional level design

# Applications of MLDesigner

- During the last 1 ½ years MLDesigner has been used for a wide area of applications, ranging from the design of global military communication systems to chip architecture design. The applications include:
  - Wireless communication systems (2G, 3G, 4G)
  - Computer board design
  - Operating system
  - Automotive electronics and networks
  - Aerospace avionics and networked operational systems
  - Optimization of production systems
  - Optimization of organizational processes

# First Results

# Company A

Integrated design flow from mission level network performance analysis to chip design

- Applications include
  - GSM/GPRS network performance analysis
  - UMTS/Edge system development
  - UMTS base station development
  - 802.11
  - Software radio

# Company B

- Design for chip for wireless communications  
UMTS, UMTS/GSM, 802.11, ...
  - Integrated modeling and simulation of hardware, operating system, software, and user application
  - Design trade offs of overall system at architecture/performance level significantly increased development speed and improved quality of design
  - Current development savings: several month
  - New department designs future systems on MLDesigner technology that integrates hardware and software (RTOS, Appl. SW).

# Company C

- The development time for a new architecture for a chip core was reduced by a factor of 3 (cycle accurate simulation at architectural/performance level). The design is now shifting to higher abstraction to achieve additional productivity improvements.
- Handoffs to chip users at performance/architectural level results in
  - Earlier handover to users
  - Much faster multi-company integrated design flow from chip design to computer

# Company D

- Development of a software system for the implementation of the ESA Packet Utilization Standard (PUS)
- Development with UML: 6 month (did not work)
- Development with MLDesigner: 10 days (worked)

# SELECTED CUSTOMERS

## 2001

SIEMENS

MOTOROLA

ROCKWELL COLLINS

## 2002

AEROSPACE CORP.

AGERE

APPLE

ASTRIUM

ERICSSON

IfEN

INFINEON

MAJOR SILICON VENDOR

KPN

LOCKHEED MARTIN

PHILIPS

## 3/2003

AIRBUS

BOEING

BOSCH

> 40 UNIVERSITIES

# MLDesigner Summary

- Covers the following simulation domains:
  - Discrete Event
  - Hierarchical Finite State Machine, including Statechart (UML) semantics
  - Synchronous Data Flow
  - Dynamic Data Flow
  - Continuous/Analog
- Covers all abstraction levels (mission level to implementation)
- Supports XML database